Faculty Development Program (FDP) on VLSI Design - Modelling & Simulation

1. **Date of the Event:** 02-1-2024 to 07-1-2024

2. **Title of the Event:** Faculty Development Program(FDP) on VLSI Design- Modelling & Simulation

3. **Objective of the Program:**

The objective of this Faculty development Program (FDP) on VLSI Design - Modelling & Simulation is to enhance the knowledge and skills of faculty members in the field of VLSI design. The program aims to provide participants with a comprehensive understanding of VLSI concepts, methodologies and tools enabling them to effectively teach and guide students in the rapidly evolving field of semi-conductor design. The program focuses on hands-on experiences and practical applications. This FDP seeks to empower educators with the latest advancements in VLSI technology, fostering research and innovation in this critical domain.

4. **Resource Persons : Dr. Kushal Kovelakonda,**
Vice President,
Chip smart Technologies Pvt Ltd.

Technical Team:

S.No	Name of the Trainer	Designation
1.	M. Bhargav Teja Senior Analog Circuit Engineer Chipsmart Technologies Pvt Ltd	Technical Team
2.	T. Anil Kumar Senior Design Verification Engineer Chipsmart Technologies Pvt Ltd	Technical Team

5. Participant Details:

S.No	Name of the Branch	No.of Faculty
1.	E.C.E	40

6. Banner of the Event:

7. Brochure of the Event :

One Week Faculty Development Programme (FDP) on

"VLSI DESIGN – MODELLING & SIMULATION"

02nd to 07th January, 2024

Registration Form

Name: _____

Designation: _____

College: _____

Department: _____

Address:

_____

_____

_____

WhatsApp Mobile No: _____

E-Mail Id: _____

Category: Academic/Industry/Others

Signature of the Participant

Date: _____ Place: _____

Participants need to register through the link mentioned below:

Registration Link

https://docs.google.com/forms/d/1OoXAgzXoEphoHlVO63rwa_OgWbJjoY6o3bRDnfYfAOU/edit

Eligibility & Registration:

Registration Fee: Rs 300/- per head.
Phone Pay/Gpay: 8019910538 (Malineni Perumallu Educational Society)
The participants to the course will be faculty and Ph.D scholars from AICTE approved technical institutions.

Mode of Conduction: ONLINE

Online meeting link will be sent to the registered WhatsApp mobile number and E-Mail Id. Since Hands-on sessions will be conducted, all the participants are requested to attend all sessions without fail.

Certification:

E-certificates will be issued to all the participants who have submitted assignments and attended all the sessions of the programme.

Chief Patron
Dr.Malineni Perumallu
Chairman,
Malineni Lakshmaiah Group of Colleges

Patron
Dr.Jetti Appa Rao
Principal

Convener
Dr.D.Vijaya Saradhi
Professor & Head, Dept of ECE
Ph:9052222407

Faculty Coordinators

Mr.T.Venkat Rao
Assoc. Prof, Dept of ECE
Ph:7396237841

Mr.Y.Bhaskara Rao
Assoc. Prof, Dept of ECE
Ph: 9032947721

MALINENI LAKSHMAIAH
WOMEN'S ENGINEERING COLLEGE
Approved by AICTE, New Delhi, Affiliated to JNTUK, Kakinada
Accredited by NBA for CSE & ECE and NAAC A+ Grade
Pulladigunta (v), Vatticherukuru(Mdl), Guntur, A.P - 522017

Faculty Development Programme on "VLSI Design – Modelling & Simulation"

02nd to 07th January, 2024

organised by

Department of ECE
Malineni Lakshmaiah Women's Engineering College

About the Institution:

Malineni Lakshmaiah Women's Engineering College (MLEW) is a premier institute established in 2008 under the patronage of the Malineni Perumallu Educational Society. The institute is comprised of, among others, the Departments of Electronics and Communication Engineering (ECE), Computer Science and Engineering (CSE), Information Technology (IT), Data Science (DS), Artificial Intelligence & Machine Learning (AIML), Artificial Intelligence & Data Science (AI&DS). The Institute also offers MCA and MBA Programs. MLEW is an autonomous institution, affiliated to JNTU, Kakinada, and is approved by AICTE. The Departments of ECE & CSE are accredited by the NBA & institute is accredited by NAAC A+ grade.

About the Department:

The Department of Electronics and Communication Engineering was established in the year 2008 with an intake of 120.

The Department is accredited by NBA in 2022 for a period of 3 years. M.Tech in VLSI system Design is also run in the department. Department has very well-equipped Labs such as Communication Lab, Micro Controller Lab, Digital Signal Processing Lab, Microwave & Optical Communication Lab, eCAD & VLSI Lab. The Department has highly qualified faculty with vast experience. The Department has a well-balanced workforce having experience in academics and in industry.

About the FDP:

This FDP is a platform for discussion on VLSI Design-Modelling and Simulation. It aims at encouraging research in the field by exposing the faculty to experts from industry and by sharing their experience and ideas with peer group. Further, it provides a platform for faculty, researchers and students to upgrade their knowledge of research and to interact with experienced researchers. The speakers will provide insights on importance of relevant areas.

Outcome of the FDP:

1.Enhanced Skills: Participants gain advanced skills in VLSI modeling and simulation techniques, enabling them to keep pace with the latest advancements in the field.

2.Updated Knowledge: FDPs often provide participants with the latest information on tools, methodologies, and technologies used in VLSI design, ensuring they stay current with industry practices.

3.Effective Teaching: Educators acquire improved pedagogical methods and materials for teaching VLSI design concepts, making their instructional approach more engaging and relevant.

4.Hands-on Experience: Practical sessions and workshops allow participants to apply modeling and simulation tools, enhancing their proficiency and confidence in using these tools in real-world scenarios.

5.Curriculum Development: Educators can update and refine their curriculum based on the latest industry trends and emerging technologies discussed during the program, ensuring their courses remain relevant and aligned with industry needs.

Course Content:

1. Hands on usage of Mentor Graphics tool to understand Custom IC design flow
2. Implementation of Digital systems
3. HDL modeling concepts
4. Design of Analog Circuits
5. FPGA based Designs
6. Hands on Lab sessions using Mentor Graphics & Xilinx

Course Instructors:

1. Trainer-1
   T .Anil Kumar Reddy
   Senior Design Verification Engineer
   Chipsmart Technologies Pvt Ltd

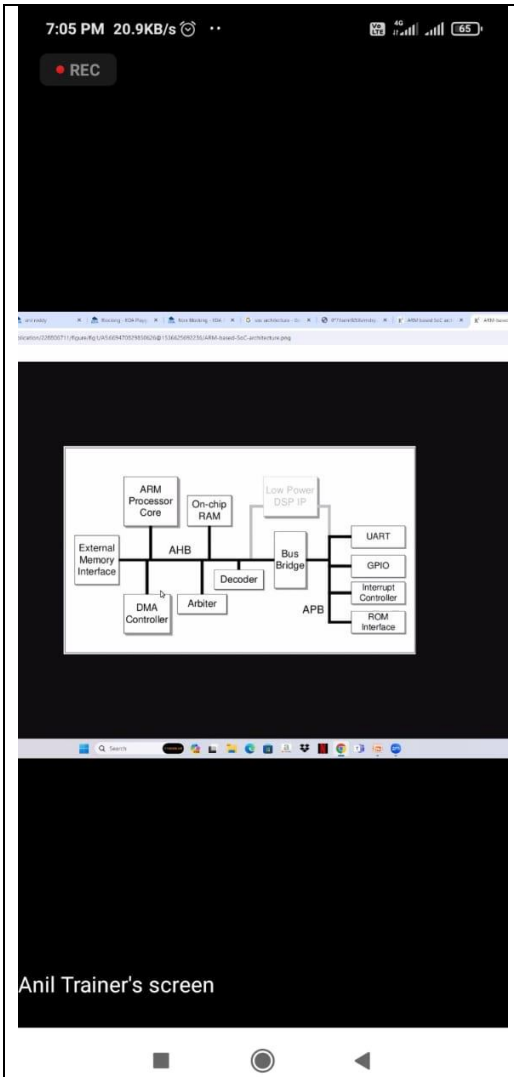
2. Trainer-2
   M. Bhargav Teja
   Senior Analog Circuit Engineer
   Chipsmart Technologies Pvt Ltd

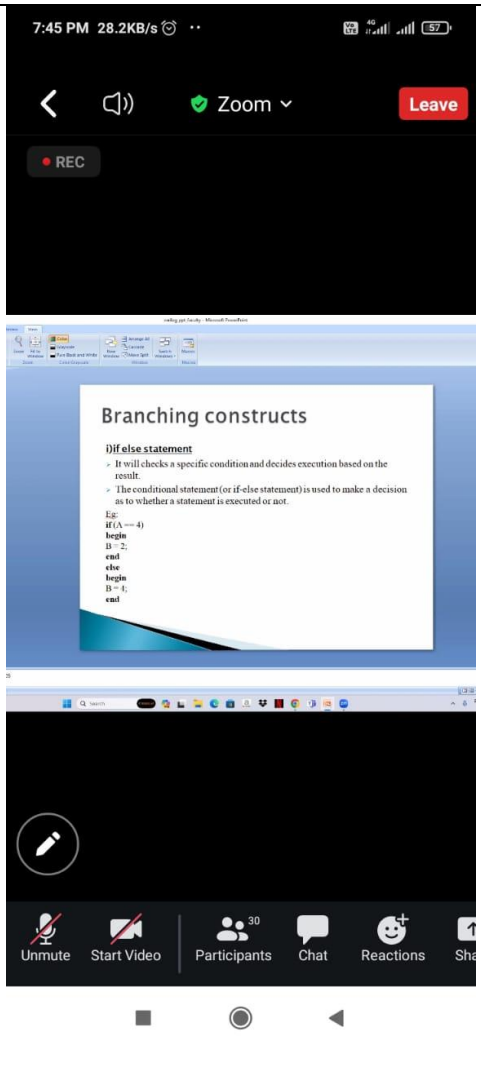
8. Schedule of the Event :

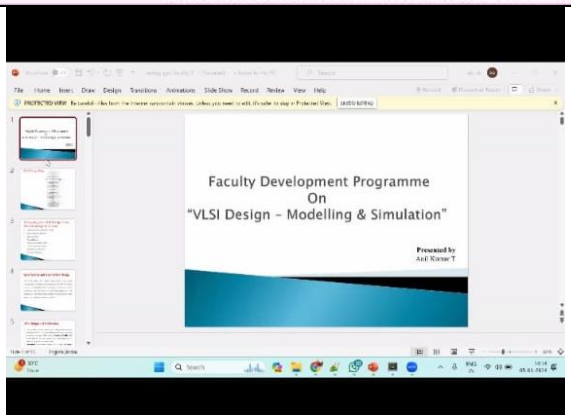
Date	Topics	Trainer
02-01-2024	MOS Device Characterizations: To determine dependence of region of operation based on I/O voltages. Extraction of basic MOS parameters, Design of Single Stage Amplifiers – Common Source, Common Drain, Common Gate Amplifiers. Analysis- DC analysis, Transient Analysis & AC analysis.	M. Bhargav Teja Senior Analog Circuit Engineer Chipsmart Technologies Pvt Ltd ***Timings:2pm to 4pm***
03-01-2024	CMOS inverter characteristics, noise margin and also the design of complex combinational logic circuit using CMOS	M. Bhargav Teja Senior Analog Circuit Engineer Chipsmart Technologies Pvt Ltd ***Timings:6pm to 8pm***
04-01-2024	Challenges and advances of field effect transistors (FETs) for future integrated circuit applications.	M. Bhargav Teja Senior Analog Circuit Engineer Chipsmart Technologies Pvt Ltd ***Timings:6pm to 8pm***
05-01-2024	Introduction to Verilog HDL, Verilog Operators and Modules, Verilog Ports, Data types and Assignments, Basics of gate level modeling, gate level modeling for some combinational circuits	T .Anil Kumar Senior Design Verification Engineer Chipsmart Technologies Pvt Ltd ***Timings:2pm to 4pm***
06-01-2024	Switch level Modeling, Modeling of CMOS gates and Boolean functions, Modeling using transmission gates, CMOS delay times	T .Anil Kumar Senior Design Verification Engineer Chipsmart Technologies Pvt Ltd ***Timings:2pm to 4pm***

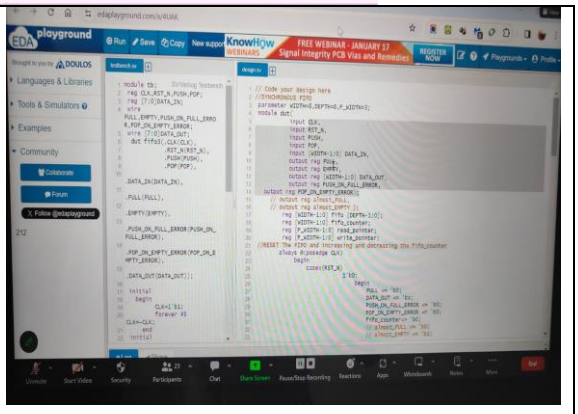
07-01-2024	Dataflow and behavioral modeling, Basics of dataflow modeling, Examples of dataflow modeling, Basics of behavioral modeling, Examples of behavioral modeling, How to write Test bench for combinational and sequential circuits	T. Anil Kumar Senior Design Verification Engineer Chipsmart Technologies Pvt Ltd ***Timings:2pm to 4pm***

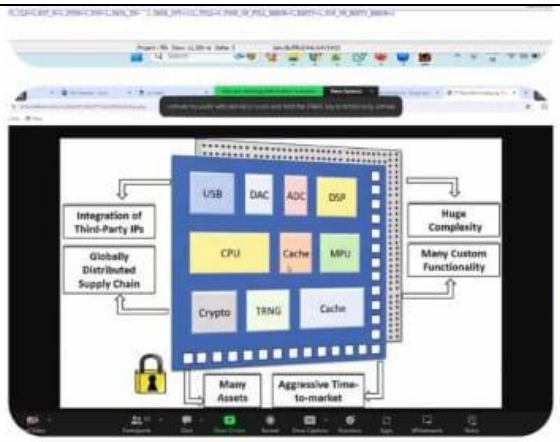
9. Event Photos:







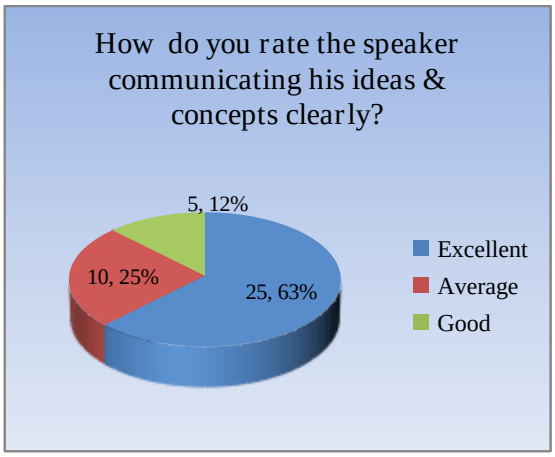


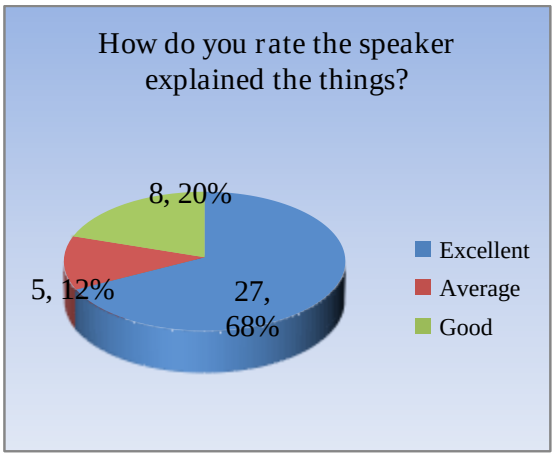


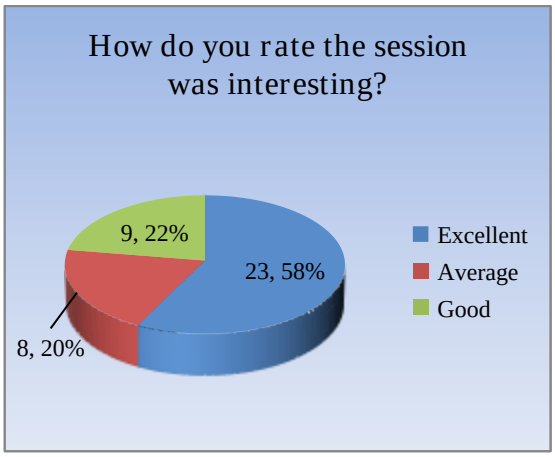
10. Social Media :

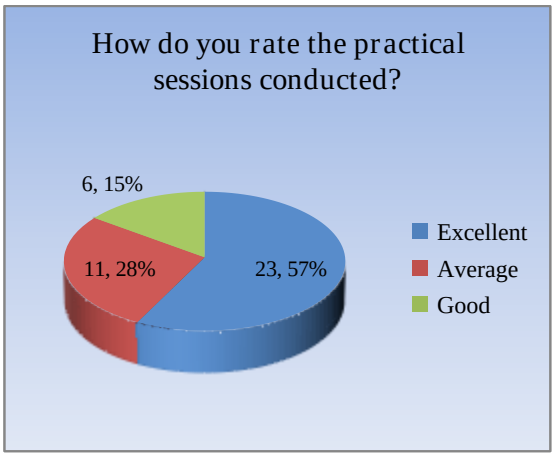
https://www.facebook.com/photo/?fbid=815716913915361&set=pcb.815717467248639&__cft__[0]=AZWuezXir9Z6To28PlB8OaDntaCOnGXy_fpFiq-z-fizLxI1cYAJ6Vr1R5DWNE8RW7A0XQgmqwD8WM6RSTuNFZrjladqvklPcIir2VZhYmrSUzKnJU6F5pkQvAkHT4E4voA&__tn__=*bH-R

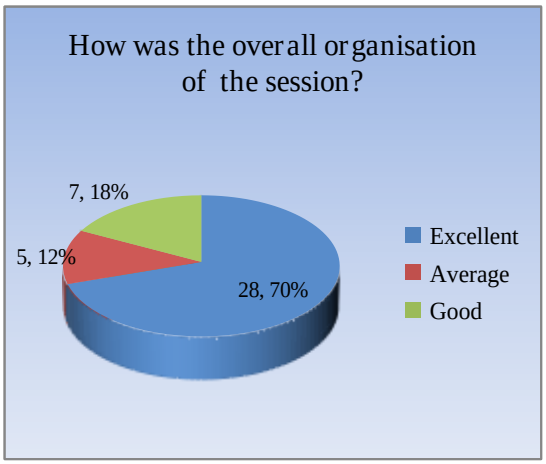
11. Participants feedback on Event:











12. Remarks:

The Faculty Development Program (FDP) on VLSI Design aimed to equip educators with advanced knowledge and skills in semiconductor design. Through a comprehensive curriculum and hands-on experiences, participants gained a deep understanding of VLSI concepts, methodologies, and tools. The program's objective was to empower faculty members to effectively teach and guide students in this rapidly evolving field, fostering research and innovation. By bridging the gap between theory and practical application, the FDP aimed to enhance the overall proficiency of educators, contributing to the growth and excellence of VLSI education and research.